WHAT IS CLAIMED IS:

1. A circuit for controlling the fly height of a disk drive read/write head assembly by controlling a current applied to a heat element resistor in the read/write head assembly, comprising:

a first voltage driver, having an output coupled to a terminal, the terminal for coupling to the heat element resistor;

a read current input for receiving a read current signal corresponding to a desired read current;

a write current input for storing a write current signal corresponding to a desired write current; and

control circuitry for coupling the read current signal and the write current signal to an input of the first voltage driver in read and write disk operations, respectively.

2. The circuit of claim 1, wherein the control circuitry comprises:

a read current register, coupled to the read current input, for storing a digital read current data value corresponding to the read current signal;

a write current register, coupled to the write current input, for storing a digital write current data value corresponding to the write current signal;

a steady-state digital-to-analog converter, having an input for receiving a digital value and an output coupled to the first voltage driver; and

select circuitry for selectively applying the read and write current data values to the input of the steady-state digital-to-analog converter in read and write disk operations, respectively.

3. The circuit of claim 2, wherein the select circuitry comprises:

a multiplexer, having an input coupled to the read current register and an input coupled to the write current register; and

control logic, having an input for receiving a read/write control signal, and having an output coupled to a control input of the multiplexer, for controlling the multiplexer responsive to the read/write control signal.

4. The circuit of claim 3, further comprising:

an overdrive transistor, having a conduction path coupled between an input of the first voltage driver and a first voltage, and having a control terminal; and

an underdrive transistor, having a conduction path coupled between an input of the first voltage driver and a second voltage, and having a control terminal;

and wherein the control logic also has outputs coupled to the control terminals of the overdrive and underdrive transistors, and is also for controlling the overdrive and underdrive transistors to conduct responsive to transitions of the read/write control signal.

5. The circuit of claim 4, further comprising:

timing circuitry, coupled to the control logic, for applying a pulse of a selected duration to the control logic;

and wherein the control logic controls the overdrive and underdrive transistors to conduct for a selected duration, responsive to the pulse from the timing circuitry.

6. The circuit of claim 4, wherein the control logic controls the overdrive transistor to conduct responsive to the read/write control signal indicating a transition from a write disk operation to a read disk operation;

and wherein the control logic controls the underdrive transistor to conduct responsive to the read/write control signal indicating a transition from a read disk operation to a write disk operation.

7. The circuit of claim 1, further comprising:

a second voltage driver, having an input and an output;

an initial state current input, coupled to an input of the second voltage driver, for receiving an initial state current signal corresponding to a desired initial state current; and

a control switch, for selectively coupling the output of the first and second voltage drivers to the terminal;

and wherein the control circuitry comprises:

control logic is also for controlling the control switch so that the output of the second voltage driver is coupled to the terminal responsive to the control logic receiving an inactive disk drive enable signal, and so that the output of the first voltage driver is coupled to the terminal responsive to the control logic receiving an active disk drive enable signal.

8. The circuit of claim 7, further comprising:

an initial state register, for storing a digital initial state current data value corresponding to the initial state current signal received at the initial state current input; and

an initial state digital-to-analog converter, having an input coupled to an output of the initial state register and an output coupled to the second voltage driver.

9. The circuit of claim 8, wherein the second voltage driver is biased by a second power supply voltage that is lower than a first power supply voltage biasing the first voltage driver.

10. The circuit of claim 1, further comprising:

circuitry for monitoring current driven from the terminal.

11. The circuit of claim 10, wherein the monitoring circuitry comprises:

a current mirror, having a control input coupled to the terminal, for generating a mirrored current corresponding to the current driven from the terminal; and

a comparator, for receiving a mirror input signal corresponding to the mirrored current, for generating a signal to the control circuitry responsive to the mirrored current.

12. The circuit of claim 11, wherein the monitoring circuitry further comprises:

limit circuitry, coupled to the comparator, for providing a limit value;

and wherein the comparator issues a fault signal responsive to a comparison of the mirror input signal to the limit value.

13. The circuit of claim 11, further comprising:

circuitry for providing a varying target voltage to the comparator;

and wherein the comparator issues a signal responsive to the mirror input signal matching the target voltage, so that the resistance of the heat element resistor can be calculated from the target voltage responsive to which the comparator issues the signal.

14. The circuit of claim 1, wherein the first voltage driver has a gain greater than unity.

15. A circuit for controlling the fly height of a plurality of disk drive read/write head assemblies by controlling a current applied to a heat element resistor in each of the plurality of read/write head assemblies, comprising:

a plurality of output voltage drive circuits, each having an input, and each having an output coupled to a corresponding one of a plurality of terminals, each of the plurality of terminals for coupling to a corresponding one of the plurality of heat element resistors;

a read current input for receiving a read current signal corresponding to a desired read current;

a write current input for storing a write current signal corresponding to a desired write current;

a demultiplexer circuit, having a first input for receiving a steady-state current signal, having a plurality of outputs, each coupled to an input of one of the plurality of output voltage drive circuits, and having at least one control input; and

control circuitry for coupling the read current signal and the write current signal to the input of the demultiplexer circuit as the steady-state current signal in read and write disk operations, respectively, and for controlling the demultiplexer circuit to apply the steady-state current signal to a selected one of the plurality of output voltage drive circuits responsive to a head select signal.

16. The circuit of claim 15, wherein the control circuitry comprises:

a read current register, coupled to the read current input, for storing a digital read current data value corresponding to the read current signal;

a write current register, coupled to the write current input, for storing a digital write current data value corresponding to the write current signal;

a steady-state digital-to-analog converter, having an input for receiving a digital value and an output coupled to the first voltage driver;

select circuitry having inputs coupled to the read and write current registers, having an output coupled to the steady-state digital-to-analog converter, and having a control input; and

control logic, having a first input for receiving a read/write control signal, and having an output coupled to the control input of the select circuitry, for controlling the select circuitry responsive to the read/write control signal, the control logic also having a second input for receiving the head select signal, and having an output coupled to the control input of the demultiplexer circuit for controlling the demultiplexer circuit responsive to the head select signal.

17. The circuit of claim 16, wherein each of the plurality of output drive circuits comprise:

a steady-state voltage driver, having an input coupled to a first input to the output drive circuit;

an initial state voltage driver, having an input coupled to a second input to the output drive circuit; and

a control switch, having a control input;

and further comprising:

an initial state register, for storing a digital initial state current data value corresponding to the initial state current signal received at the initial state current input; and

an initial state digital-to-analog converter, having an input coupled to an output of the initial state register and an output coupled to a second input to the demultiplexer circuit;

wherein the demultiplexer circuit has a plurality of outputs coupled to the first and second inputs of the plurality of output voltage drive circuits;

and wherein the control logic is also coupled to the control inputs of each of the control switches in the plurality of output drive circuits, so that the control switch in the selected one of the plurality of output voltage drive circuits couples the steady-state voltage driver to its corresponding terminal, and so that the control switch in each of the unselected ones of the plurality of output voltage drive circuits couples the initial state voltage driver to its corresponding terminal.

18. A method of controlling the fly height of a read/write head assembly in a disk drive, comprising:

connecting a first terminal to a first heat element resistor in a first read/write head assembly;

during at least a portion of a disk read operation, applying a first voltage to the first terminal; and

during at least a portion of a disk write operation, applying a second voltage to the first terminal.

19. The method of claim 18, further comprising:

storing a read current value;

storing a write current value;

wherein the step of applying the first voltage comprises:

responsive to receiving a disk read enable signal, applying a signal corresponding to the read current value to a first voltage driver, the first voltage driver having an output coupled to the first terminal;

and wherein the step of applying the second voltage comprises:

responsive to receiving a disk write enable signal, applying a signal corresponding to the write current value to the first voltage driver.

20. The method of claim 18, wherein the disk read enable signal and disk write enable signals correspond to logic levels at a read/write enable terminal;

and further comprising:

responsive to detecting a first logic level transition at the read/write enable terminal, coupling an underdrive voltage to the first voltage driver; and

responsive to detecting a second logic level transition at the read/write enable terminal, coupling an overdrive voltage to the first voltage driver.

21. The method of claim 20, wherein the first logic level transition corresponds to a transition from a disk read operation to a disk write operation;

and wherein the second logic level transition corresponds to a transition from a disk write operation to a disk read operation.

22. The method of claim 18, further comprising:

monitoring a mirrored current corresponding to current driven at the first terminal.

23. The method of claim 22, wherein the monitoring step comprises:

comparing the mirrored current to a limit value; and

responsive to the mirrored current exceeding the limit value, issuing a fault signal.

24. The method of claim 19, wherein the disk drive includes a plurality of read/write head assemblies;

and further comprising:

connecting a plurality of terminals to corresponding ones of a plurality of heat element resistors, each heat element resistor in a corresponding one of the plurality of read/write head assemblies; and

receiving a head select signal indicating a selected one of the plurality of read/write head assemblies;

wherein the steps of applying a first voltage and of applying a second voltage to a first terminal are performed responsive to the head select signal indicating selection of the first read/write assembly is selected.

25. The method of claim 24, further comprising, responsive to the head select signal indicating selection of a second read/write head assembly:

during at least a portion of a disk read operation, applying a first voltage to the second terminal; and

during at least a portion of a disk write operation, applying a second voltage to the second terminal.

26. The method of claim 25, further comprising:

for each of the plurality of read/write head assemblies indicated by the head select signal as not selected, applying an initial state voltage to its corresponding terminal.

27. The method of claim 18, further comprising:

responsive to receiving a signal indicating that the disk drive is not selected, applying an initial state voltage to the first terminal.

* * * * *